T080320 * 6026260

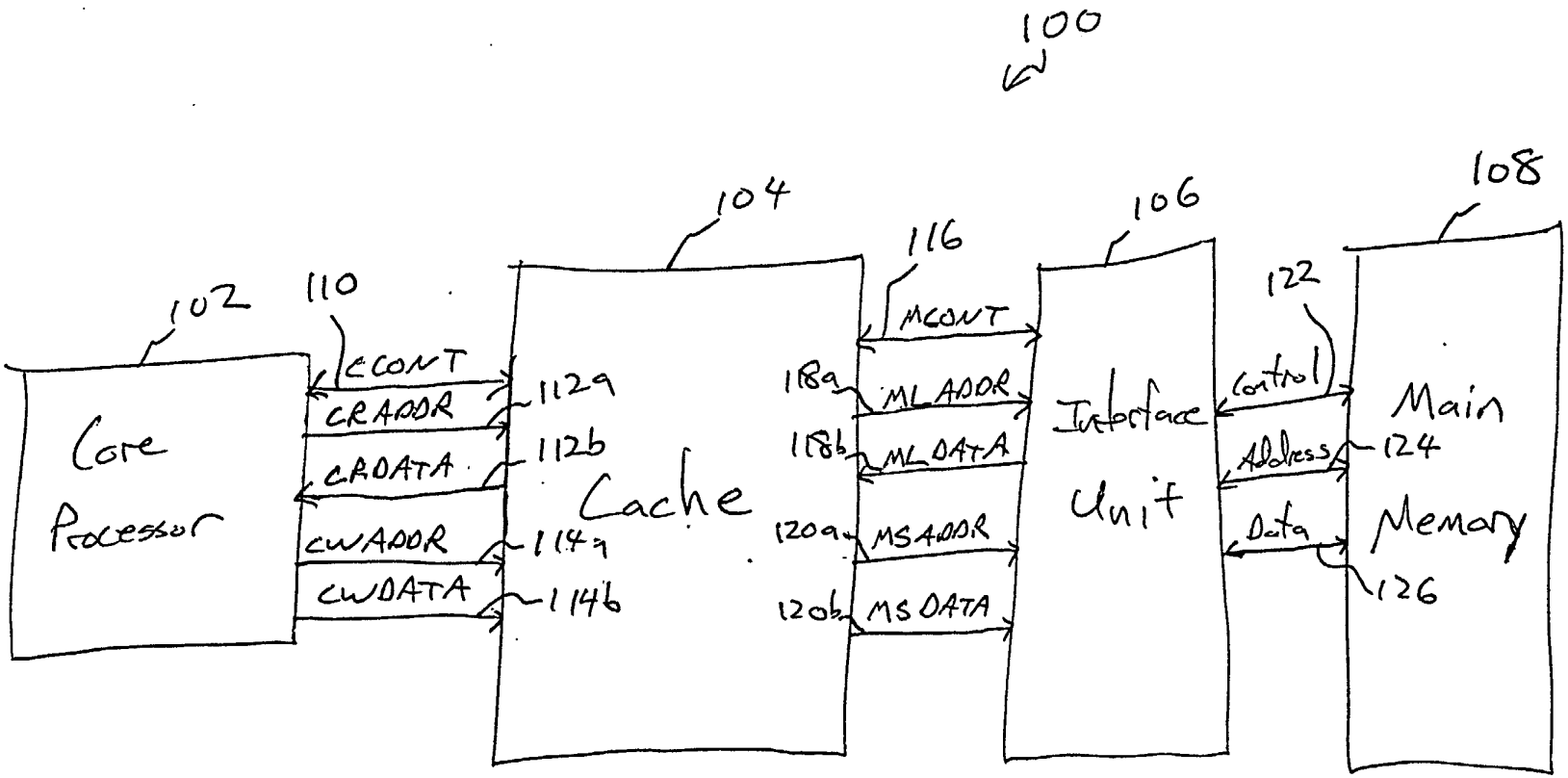

Fig. 1 (PRIOR ART)

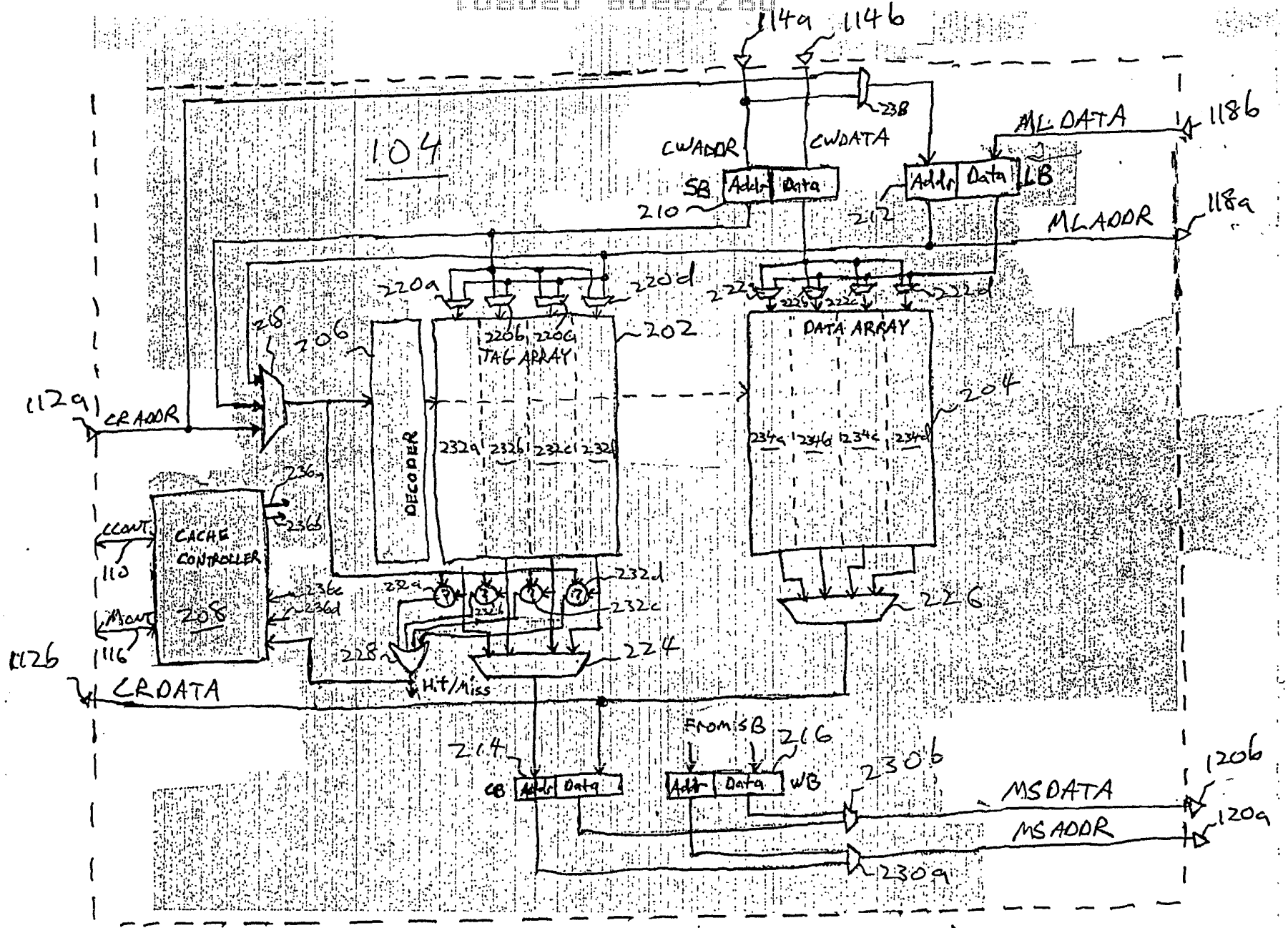

Fig. 2 (Prior Art)

TOSOZO 6026760

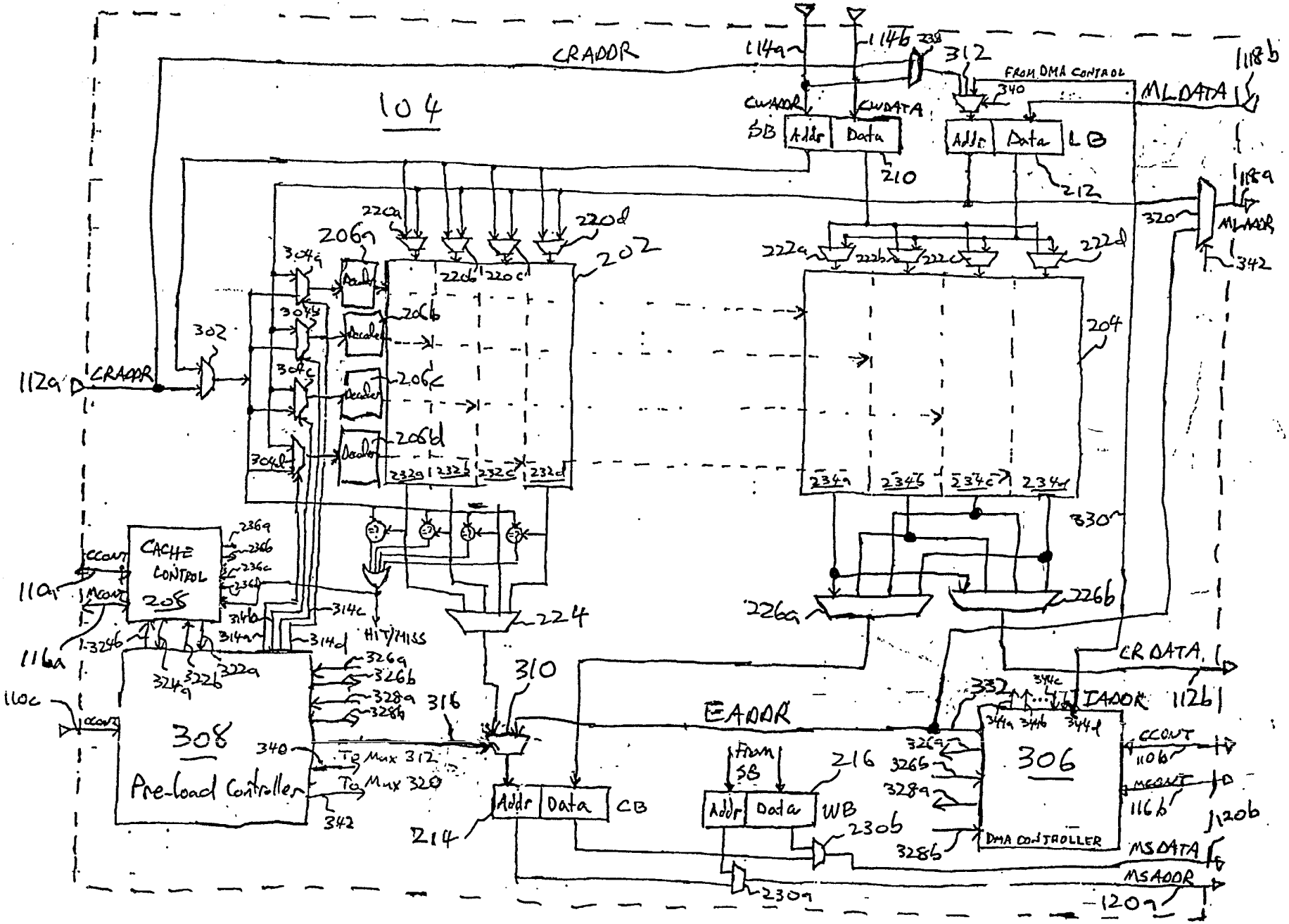

Fig. 3

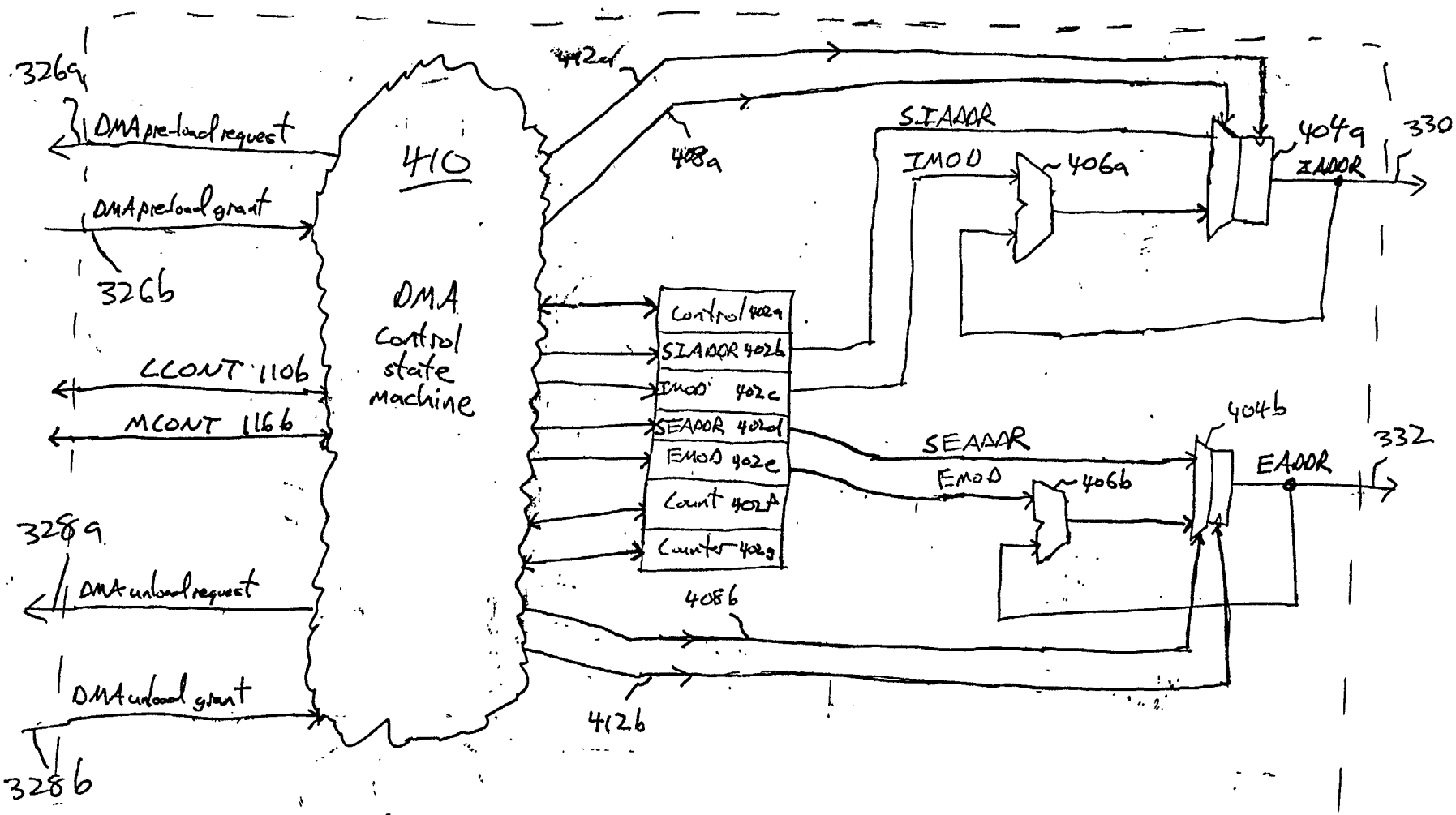
326a
DMA preload request
DMA preload grant
326b
CCONT 1106
MCONT 1166
328a
DMA unload request
DMA unload grant
328b
410
DMA control state machine
412a
408a
Control 402a
SIADDR 402b
IMOD 402c
SEADDR 402d
EMOD 402e
Count 402f
Counter 402g
408b
412b
SIADDR
IMOD
406a
404a
330
IADDR
404b
SEADDR
EMOD
406b
332
EADDR
306
DMA Controller

Fig. 4

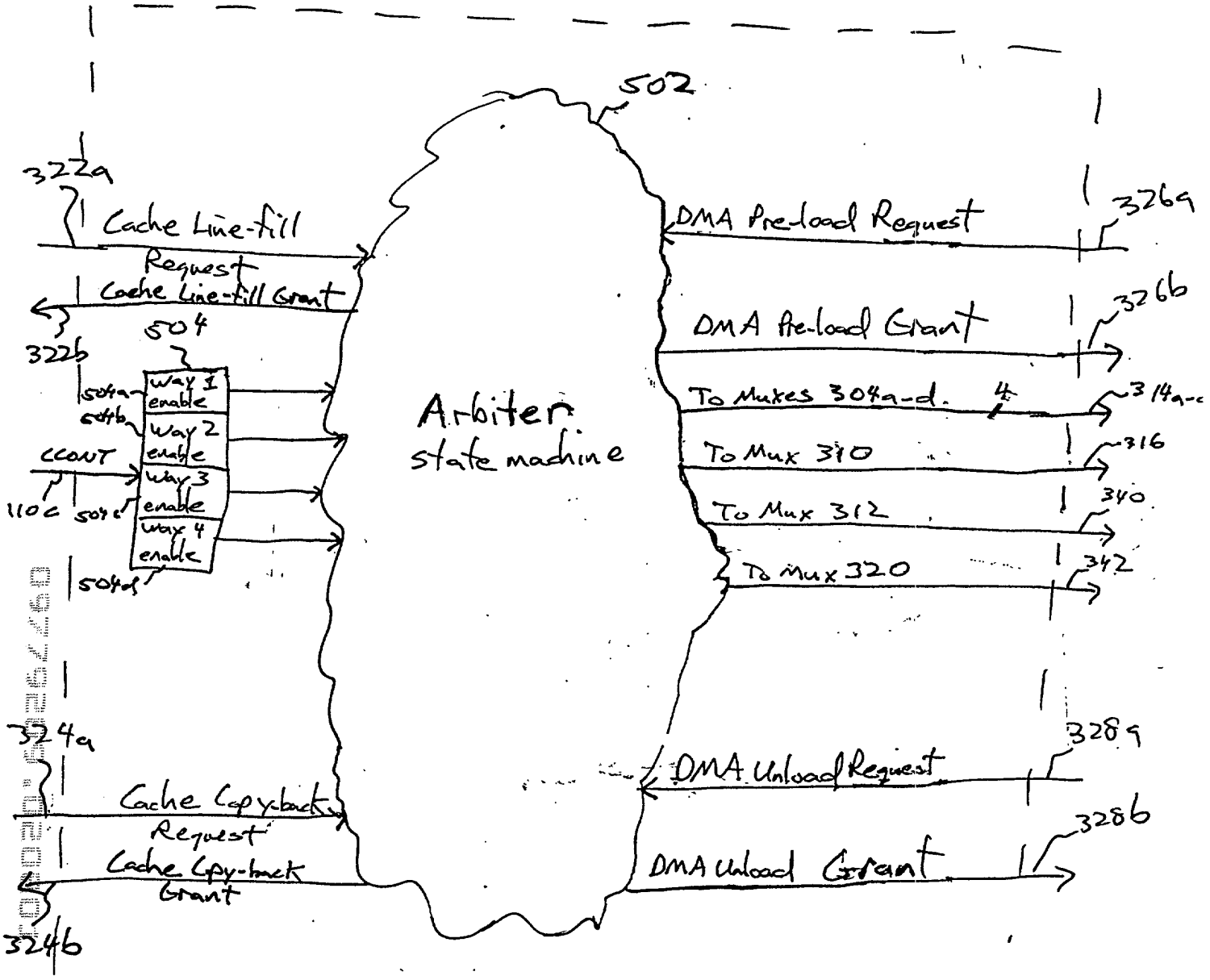
502
322a
Cache Line-fill Request
Cache Line-fill Grant
322b
504
Way 1 enable
Way 2 enable
Way 3 enable
Way 4 enable
504a
504b
CCOUT
110c
504c
504d
Arbiter state machine
DMA Pre-load Request
326a
DMA Pre-load Grant
326b
To Muxes 304a-d.
4
314a-d
To Mux 310
316
To Mux 312
340
To Mux 320
342
324a
Cache Copy-back Request
Cache Copy-back Grant
324b
DMA Unload Request
328a
DMA Unload Grant
328b
306
Pre-load Controller

Fig. 5

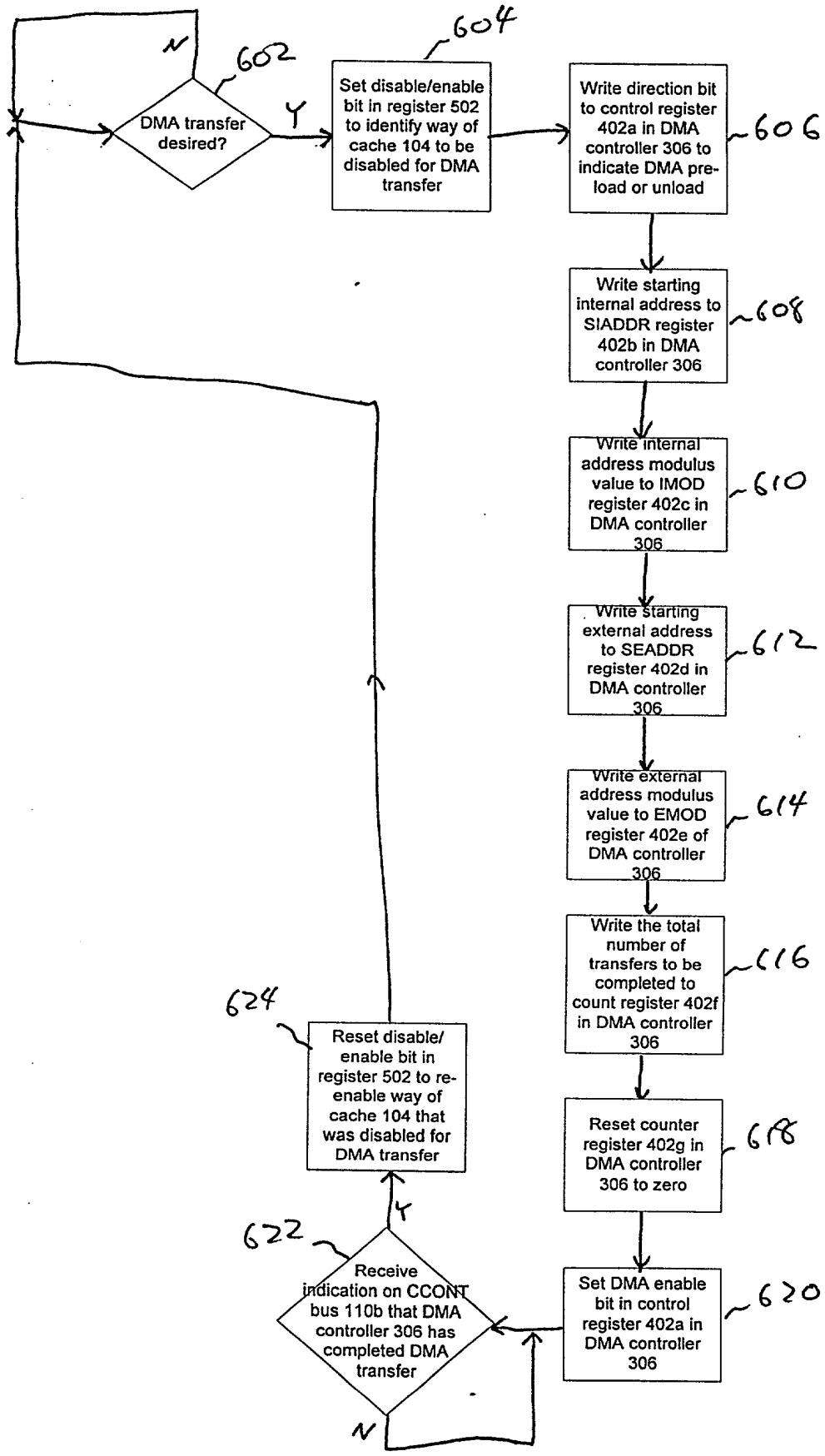
600
602
DMA transfer desired?
N
Y
604
Set disable/enable bit in register 502 to identify way of cache 104 to be disabled for DMA transfer
606
Write direction bit to control register 402a in DMA controller 306 to indicate DMA pre-load or unload
608
Write starting internal address to SIADDR register 402b in DMA controller 306
610
Write internal address modulus value to IMOD register 402c in DMA controller 306
612
Write starting external address to SEADDR register 402d in DMA controller 306
614
Write external address modulus value to EMOD register 402e of DMA controller 306
616
Write the total number of transfers to be completed to count register 402f in DMA controller 306
618
Reset counter register 402g in DMA controller 306 to zero
620
Set DMA enable bit in control register 402a in DMA controller 306
622
Receive indication on CCONT bus 110b that DMA controller 306 has completed DMA transfer
624
Reset disable/ enable bit in register 502 to re-enable way of cache 104 that was disabled for DMA transfer

Fig. 6

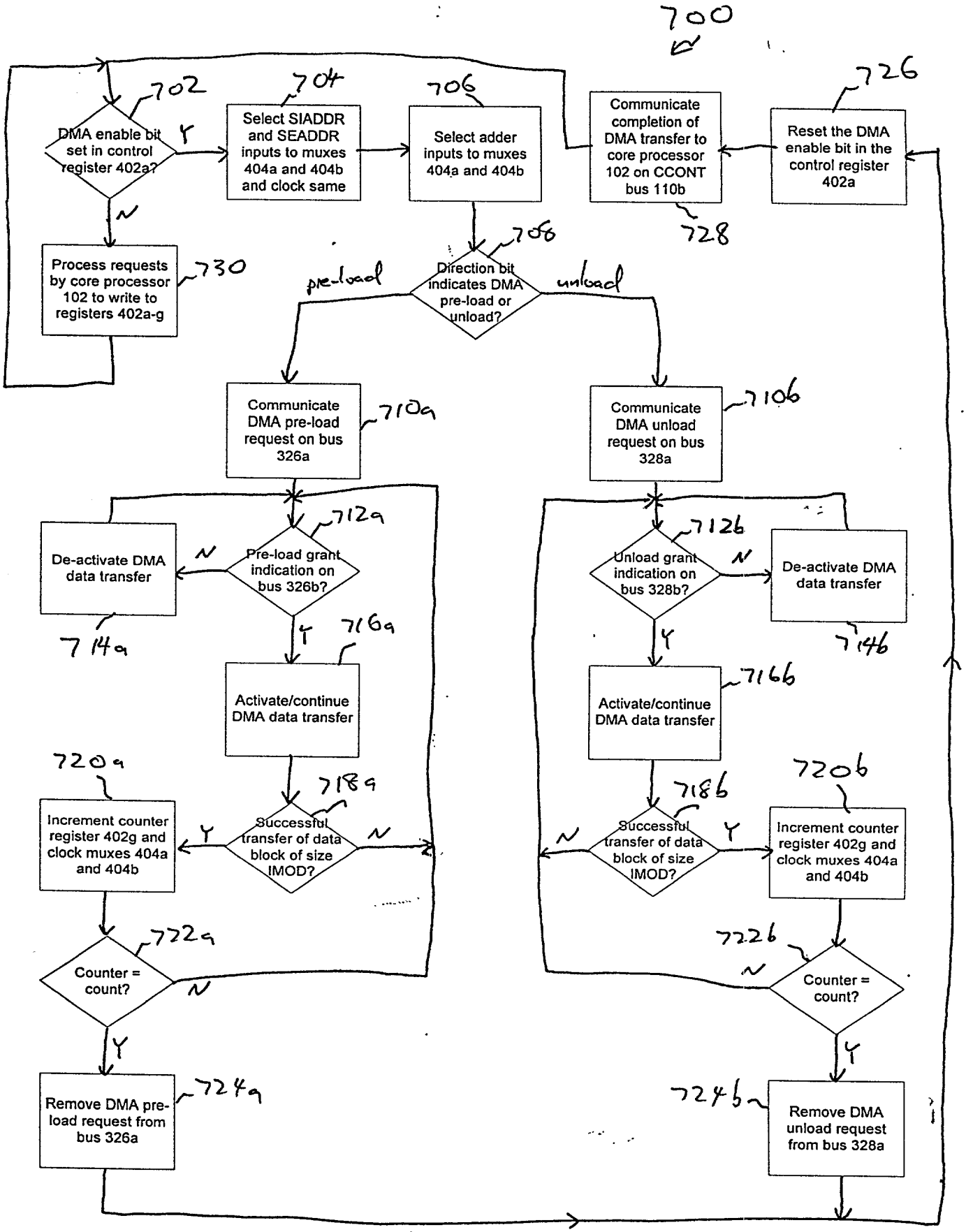
700
702
DMA enable bit set in control register 402a?
Y
N
704
Select SIADDR and SEADDR inputs to muxes 404a and 404b and clock same
706
Select adder inputs to muxes 404a and 404b
726
Reset the DMA enable bit in the control register 402a
Communicate completion of DMA transfer to core processor 102 on CCONT bus 110b
728
Process requests by core processor 102 to write to registers 402a-g
730
706
Direction bit indicates DMA pre-load or unload?
pre-load
unload
Communicate DMA pre-load request on bus 326a
710a
Communicate DMA unload request on bus 328a
710b
712a
Pre-load grant indication on bus 326b?
N
Y
De-activate DMA data transfer
714a
716a
Activate/continue DMA data transfer
712b
Unload grant indication on bus 328b?
N
Y
De-activate DMA data transfer
714b
716b
Activate/continue DMA data transfer
720a
Increment counter register 402g and clock muxes 404a and 404b
718a
Successful transfer of data block of size IMOD?
Y
N
718b
Successful transfer of data block of size IMOD?
N
Y
720b
Increment counter register 402g and clock muxes 404a and 404b
722a
Counter = count?
N
Y
722b
N
Counter = count?
Y
724a
Remove DMA pre-load request from bus 326a
724b
Remove DMA unload request from bus 328a

Fig. 7

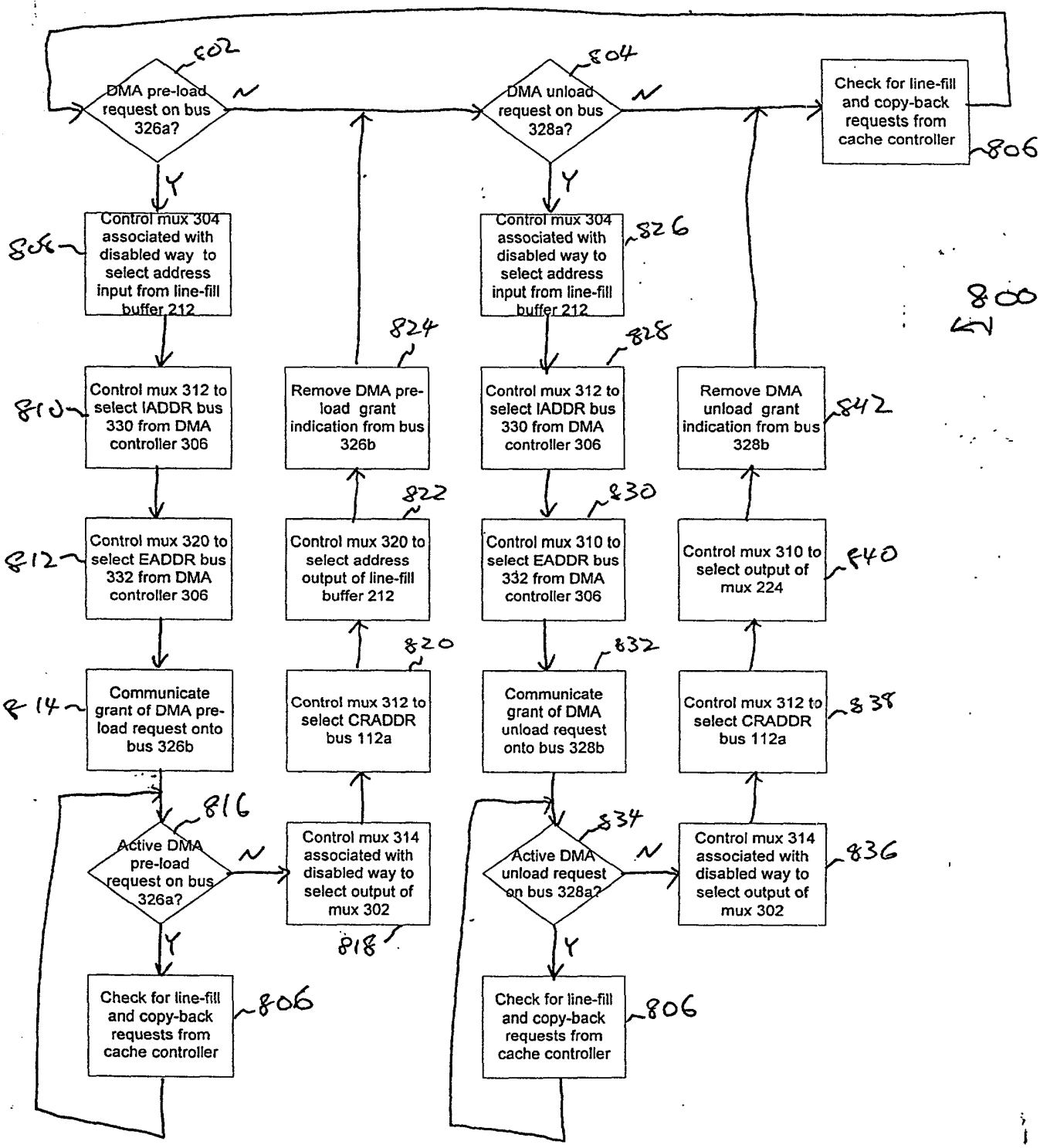
802
DMA pre-load request on bus 326a?
N
Y
804
DMA unload request on bus 328a?
N
Y
Check for line-fill and copy-back requests from cache controller
806
800
808
Control mux 304 associated with disabled way to select address input from line-fill buffer 212
826
Control mux 304 associated with disabled way to select address input from line-fill buffer 212
810
Control mux 312 to select IADDR bus 330 from DMA controller 306
824
Remove DMA pre-load grant indication from bus 326b
828
Control mux 312 to select IADDR bus 330 from DMA controller 306
842
Remove DMA unload grant indication from bus 328b
812
Control mux 320 to select EADDR bus 332 from DMA controller 306
822
Control mux 320 to select address output of line-fill buffer 212
830
Control mux 310 to select EADDR bus 332 from DMA controller 306
840
Control mux 310 to select output of mux 224
814
Communicate grant of DMA pre-load request onto bus 326b
820
Control mux 312 to select CRADDR bus 112a
832
Communicate grant of DMA unload request onto bus 328b
838
Control mux 312 to select CRADDR bus 112a
816
Active DMA pre-load request on bus 326a?
N
Y
Control mux 314 associated with disabled way to select output of mux 302
818
834
Active DMA unload request on bus 328a?
N
Y
Control mux 314 associated with disabled way to select output of mux 302
836
Check for line-fill and copy-back requests from cache controller
806
Check for line-fill and copy-back requests from cache controller
806

Fig. 8A

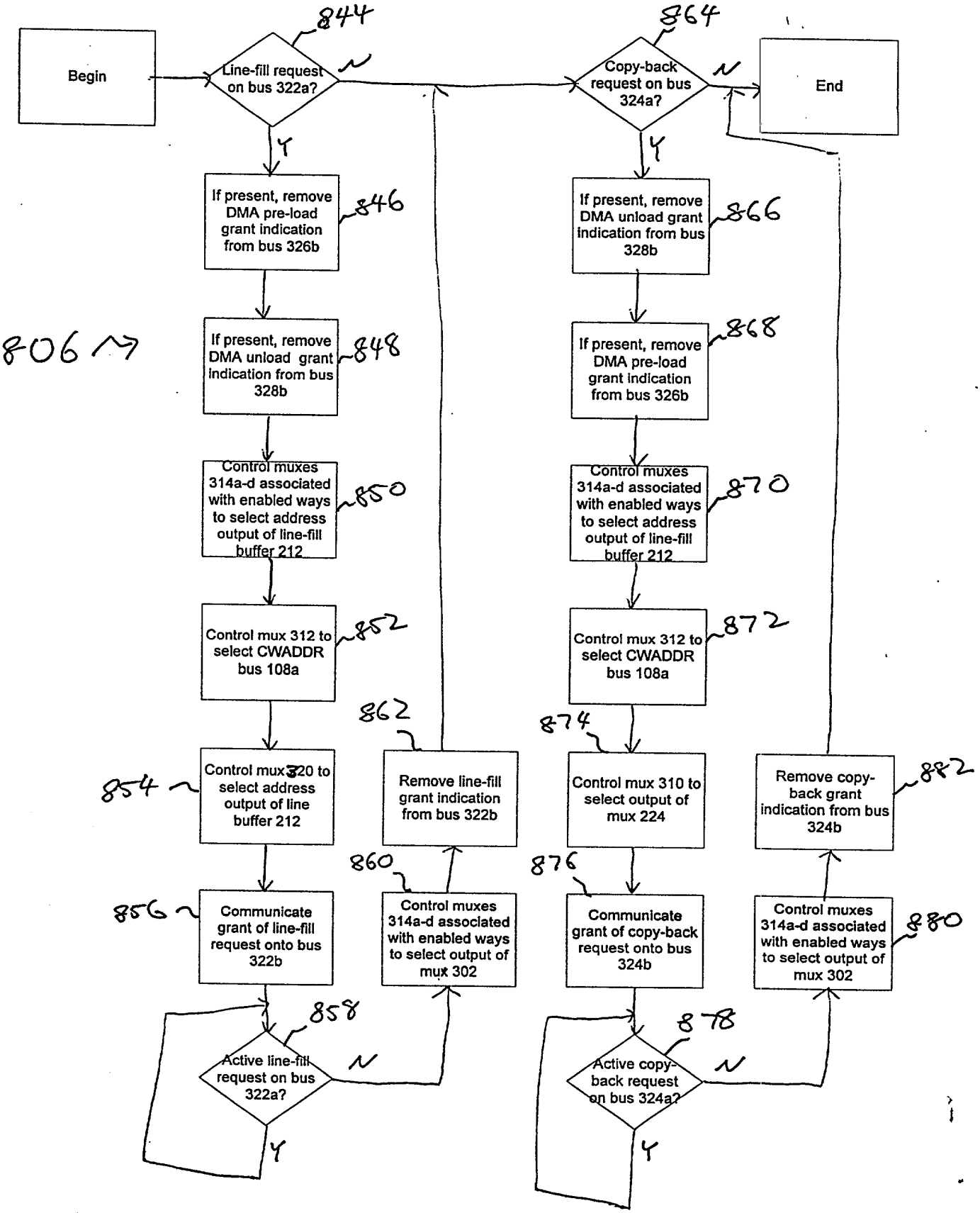
Begin
Line-fill request on bus 322a?
844
Y
N
If present, remove DMA pre-load grant indication from bus 326b
846
If present, remove DMA unload grant indication from bus 328b
848
Control muxes 314a-d associated with enabled ways to select address output of line-fill buffer 212
850
Control mux 312 to select CWADDR bus 108a
852
Control mux 320 to select address output of line buffer 212
854
Communicate grant of line-fill request onto bus 322b
856
Active line-fill request on bus 322a?
858
Control muxes 314a-d associated with enabled ways to select output of mux 302
860
Remove line-fill grant indication from bus 322b
862
Copy-back request on bus 324a?
864
End
If present, remove DMA unload grant indication from bus 328b
866
If present, remove DMA pre-load grant indication from bus 326b
868
Control muxes 314a-d associated with enabled ways to select address output of line-fill buffer 212
870
Control mux 312 to select CWADDR bus 108a
872
Control mux 310 to select output of mux 224
874
Communicate grant of copy-back request onto bus 324b
876
Active copy-back request on bus 324a?
878
Control muxes 314a-d associated with enabled ways to select output of mux 302
880
Remove copy-back grant indication from bus 324b
882
806

Fig. 8B

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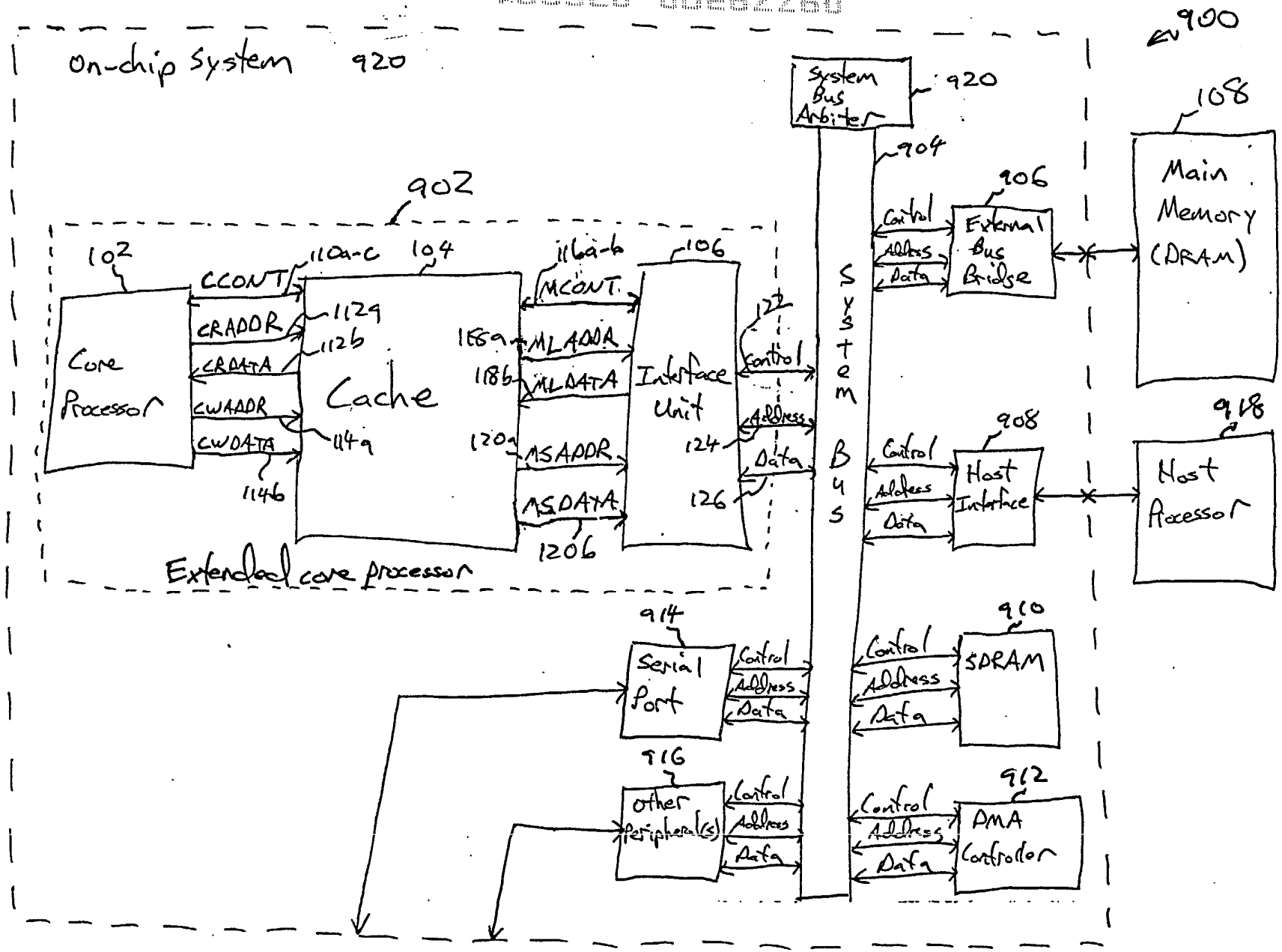

Fig. 9